AMENDMENTS TO THE CLAIMS

1-18 (Canceled)

19. (Currently amended) Circuit configuration for storing data words in a RAM module, comprising:

a first circuit unit for generating a check bit word from at least one data word when writing and reading the at least one data word,

a plurality of registers for the allocated storage of check bit words for the data words, and

a second circuit unit by means of which, when reading data words, the associated check bit word is compared to the check bit word regenerated by the first circuit unit, and for generating an error message if the check bit words do not correspond,

wherein the number of registers in said plurality of registers is determined by including one CRC register for each four data words,

further including a multiplexer for storing four data words as one memory word, and a CRC arithmetic unit for calculating the CRC word from a memory word and for storing the CRC word in an associated CRC register.

20. (Previously presented) Circuit configuration as claimed in claim 19, wherein the number of registers in said plurality of registers is determined by including one 2-bit parity register for each data word.

21 – 22 (Canceled)

23. (Currently amended) Circuit configuration as claimed in claim [22]19, wherein the data words are 32 bits long and the CRC words are 9 bits long.

24. (Previously presented) Circuit configuration as claimed in claim 19, further including a global check bit word register for storing a global check bit word, the bits of which are respectively determined from equal digits of all data words, and an associated register for storing a check bit word which is determined from the contents of the global register.

25. (New) Circuit configuration for storing data words in a RAM module, comprising:

a first circuit unit for generating a check bit word from at least one data word when writing and reading the at least one data word,

a plurality of registers for the allocated storage of check bit words for the data words, and

a second circuit unit by means of which, when reading data words, the associated check bit word is compared to the check bit word regenerated by the first circuit unit, and for generating an error message if the check bit words do not correspond,

a global check bit word register for storing a global check bit word, the bits of which are respectively determined from equal digits of all data words, and an associated register for storing a check bit word which is determined from the contents of the global register.